DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7 recite the limitation "the first mono-crystalline emitter" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim, since the parent claim recites "a mono-crystalline emitter" in line 1 and "a highly doped first mono-crystalline layer" in line 4, but does not recite "a first mono-crystalline emitter." This limitation therefore renders the claim indefinite.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 5, 8, 9, 11, 12, 15, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda (US 6, 482, 710) in view of Sato (US 2004/0056274).

Regarding claim 1, Oda discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench (Fig.4B) formed on

a silicon substrate (Fig.4B, numeral 2) having opposed silicon oxide side walls (Fig.4B, numeral 11); selectively growing a highly doped first mono-crystalline layer (Fig.4C, numeral 13; column 8, lines 57-60) on the silicon substrate (Fig.4C, numeral 2) in the trench; forming a polysilicon layer (Fig.5C, numeral 19) over the silicon oxide side walls (Fig.5C, numeral 11); and forming a second mono-crystalline layer (Fig.5A, numeral 14; column 7, lines 39-45) over the first mono-crystalline layer (Fig.5A, numeral 13); wherein the polysilicon layer is formed by non-selectively growing a second silicon layer over the trench (Fig.5C, numeral 19)

Oda does not disclose that the second mono-crystalline layer is formed by non-selectively growing a second silicon layer over the trench.

Sato however discloses forming a mono-crystalline layer (Fig.5E, numeral 9a, [0056]) by non-selectively growing a second silicon layer over the trench (Fig.5E, numeral 9; [0055]; [0086]).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Oda with Sato to form the second mono-crystalline layer by non-selectively growing a second silicon layer over the trench for the purpose of improving transistor characteristics (Sato, [0067]).

Regarding claim 8, Oda discloses a method for forming a highly n-type doped layer in a semiconductor wafer, comprising: providing a first active region comprised of a silicon substrate (Fig. 4A, numeral 12); providing a second region comprised of silicon oxide (Fig.4A, numeral 11); selectively growing a highly doped first mono-crystalline layer on the silicon substrate (Fig.4C, numeral 13);

and forming a polysilicon layer over the silicon oxide (Fig.5C, numeral 19); and forming a second mono-crystalline layer (Fig.5A, numeral 14) over the highly doped mono-crystalline layer (Fig. 5A, numeral 13) wherein the polysilicon layer is formed by non-selectively growing a second silicon layer over the first active region and the second region (Fig.5C, numeral 19).

Oda does not disclose that the second mono-crystalline layer is formed by non-selectively growing a second silicon layer over the trench.

Sato however discloses forming a mono-crystalline layer (Fig.5E, numeral 9a, [0056]) by non-selectively growing a second silicon layer over the trench (Fig.5E, numeral 9; [0055]; [0086]).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Oda with Sato to form the second mono-crystalline layer by non-selectively growing a second silicon layer over the trench for the purpose of improving transistor characteristics (Sato, [0067]).

Regarding claim 15, Oda discloses a method for growing a mono-crystalline emitter for a bipolar transistor, comprising: providing a trench formed on a substrate having opposed silicon oxide side walls (Fig.4B, numeral 11); growing a highly doped layer on the substrate in the trench using selective epitaxial growth (Fig. 4C, numeral 13; column 8, lines 57-65); forming a polysilicon layer over the silicon oxide side walls (Fig.5C, numeral 19); and forming a mono-crystalline layer (Fig.5A, numeral 14) over the highly doped layer (Fig.5A, numeral 13).

Oda does not disclose that the polysilicon layer and the second mono-crystalline layer are formed by growing a second layer over the trench using differential epitaxial growth.

Sato however discloses forming a mono-crystalline layer (Fig.5E, numeral 9a, [0056]) and the polysilicon layer (Fig.4A, numeral 9B) by growing a second silicon layer over the trench (Fig.5E, numeral 9; [0055]; [0086]) using differential epitaxial growth ([0056]; note: bottom portion (9a) is a single-crystal, while sidewall portion (9b) is a polycrystal).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Oda with Sato to form the polysilicon layer and the second mono-crystalline layer by growing a second silicon layer over the trench using differential epitaxial growth for the purpose of improving transistor characteristics (Sato, [0067]).

Regarding claims 2 and 9, Oda discloses that the step of selectively growing a highly doped first mono-crystalline layer is accomplished using selective epitaxial growth (column 8, lines 57-67).

Regarding claims 4 and 11, Sato discloses that the step of non-selectively growing the second silicon layer is accomplished using differential epitaxial growing ([0056]; note: bottom portion (9a) is a single-crystal, while sidewall portion (9b) is a polycrystal).

Regarding claims 5, 12, and 17, Oda discloses that the first mono-crystalline layer is substantially grown only on active area on the silicon substrate (Fig.4C, numeral 13).

5. Claims 3, 10, and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Oda and Sato as applied to claims 1, 8, and 15 above, and further in view of Koshimizu (US 2005/0181569).

Regarding claims 3, 10, and 16, Oda in view of Sato discloses all limitations of claims 1, 8, and 15 for reasons above.

Oda in view of Sato does not disclose the selective epitaxial growth using a precursor from the group consisting of: SiH_2Cl_2, SiH_4, $SiCl_4$, $SiCl_3$, Si_2H_6, Si_3H_8, GeH_4, and SiH_3CH_3.

Using the above precursors in selective epitaxial growth however is well-known in the art. Koshimizu, for example, discloses the selective epitaxial growth using the above precursors ([0056]).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to use a precursor from the group consisting of: SiH_2Cl_2, SiH_4, $SiCl_4$, $SiCl_3$, Si_2H_6, Si_3H_8, GeH_4, and SiH_3CH_3 for the purpose of selectively depositing silicon or germanium containing film.

6. Claims 6, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda and Sato as applied to claims 1, 8, and 15 above, and further in view of Verma (US 2005/0079678).

Regarding claims 6, 13, and 18, Oda in view of Sato discloses all limitations of claims 1, 8, and 15 above.

Oda in view of Sato does not disclose performing a salicidation process using a silicide selected from the group consisting of: titanium, cobalt, and nickel.

Verma however discloses a method comprising performing a salicidation process using a silicide (Fig. 9, (904,905, 906)) selected from the group consisting of: titanium, cobalt, and nickel ([0070]) in order to fabricate a heterojunction bipolar transistor (Abstract).

It would have been obvious to one skilled in the art to modify the method of Oda and Sato by performing a salicidation process using a silicide selected from the group consisting of titanium, cobalt, and nickel for the purpose of fabricating bipolar transistor.

7. Claims 7, 14, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oda and Sato as applied to claims 1, 8, and 15 above, and further in view of Frei (US 6,509,242).

Regarding claim 7, Oda in view of Sato does not disclose that the first mono-crystalline emitter is n-type doped with an element selected form the group consisting of phosphorous and arsenic.

Frei however discloses a method wherein the first mono-crystalline emitter is n- type doped with an element selected from the group consisting of: phosphorous and arsenic (Column 3, lines 49-53) in order to fabricate a heterojunction bipolar emitter (Abstract).

It would have been therefore obvious to one skilled in the art at the time of the invention to modify Oda with Frei to perform n-type doping the first mono-crystalline emitter with an element selected from the group consisting of: phosphorous or arsenic in order to fabricate a heterojunction bipolar emitter.

Regarding claim 14, Oda in view of Sato does not disclose that the highly n-typed doped layer is doped with an element selected form the group consisting of phosphorous and arsenic.

Frei however discloses a method wherein the n-typed doped layer is doped with an element selected from the group consisting of: phosphorous and arsenic (Column 3, lines 49-53) in order to fabricate a heterojunction bipolar emitter (Abstract).

It would have been therefore obvious to one skilled in the art at the time of the invention to modify Oda with Frei to perform n-type doping the first mono-crystalline emitter with an element selected from the group consisting of: phosphorous or arsenic in order to fabricate a heterojunction bipolar emitter.

Regarding claim 19, Oda in view of Sato does not disclose that the mono-crystalline emitter is n-type doped with an element selected form the group consisting of phosphorous and arsenic.

Frei however discloses a method wherein the first mono-crystalline emitter is n- type doped with an element selected from the group consisting of: phosphorous and arsenic (Column 3, lines 49-53) in order to fabricate a heterojunction bipolar emitter (Abstract).

It would have been therefore obvious to one skilled in the art at the time of the invention to modify Oda with Frei to perform n-type doping the first mono-crystalline emitter with an element selected from the group consisting of: phosphorous or arsenic in order to fabricate a heterojunction bipolar emitter.

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oda and Sato as applied to claim 15 above, and further in view of Asai (US Patent 6,455,364).

Regarding claim 20, Oda in view of Sato does not disclose that the mono-crystalline emitter is p-type doped using boron.

Asai however discloses a method wherein the first mono-crystalline emitter (Fig. 1, (111)) is p-type doped using boron Column 12, lines 3-21) in order fabricate a hetero bipolar transistor and a SiGe-BiCMOS device (Column 7, lines 24-28).

It would have been obvious to one skilled in the art at the time of the invention to modify Oda with Asai to perform by p-type doping the mono-crystalline emitter with boron in order to fabricate a hetero bipolar transistor and a SiGe BiCMOS device.

Response to Arguments

9. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is

filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Keisha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
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